

AMENDMENTS TO THE CLAIMS

Claim 1 (canceled)

- 5 Claim 2 (currently amended): ~~The integrated circuit of claim 1 further comprising~~
An integrated circuit adapted for supporting a processor, the integrated circuit
comprising:

an input line for indicating a type of said processor;

a plurality of input lines for indicating a programmable core voltage requested

10 by said processor;

a plurality of input lines for indicating a default core voltage of said processor;

an input line for indicating a sleep state of said processor;

a plurality of input lines for indicating a processor operating frequency;

a plurality of power signal input lines;

15 a plurality of output lines for providing a Frequency-Identification value to a

North Bridge chipset or a South Bridge chipset, said

Frequency-Identification value corresponding to an operating frequency of
said processor;

20 a plurality of output lines for overriding an internal Frequency-Identification code
of said processor; and

a power detection circuit for determining suitability of electrical power provided
by a power regulator according to said power signal input lines and providing
an associated Power-Good signal line.

- 25 Claim 3 (original): The integrated circuit of claim 2 further comprising:

a programmable Voltage-Identification override table;

a programmable Frequency-Identification override table;

a serial data input line for programming said Voltage-Identification override
table and said Frequency-Identification override table; and

- 30 a plurality of output lines for passing a Voltage-Identification value to said
power regulator

Claim 4 (original): The integrated circuit of claim 3 further comprising a plurality of default sleep Voltage-Identification lines corresponding to a default sleep voltage for said processor.

- 5 Claim 5 (original): The integrated circuit of claim 4 further comprising a Voltage-Identification logic circuit for generating said Voltage-Identification value, said Voltage-Identification logic circuit comprising:
- 10 a desktop Voltage-Identified multiplexer for generating a DKTP value from said input lines for indicating a default core voltage of said processor and said default sleep Voltage-Identification lines according to said input line for indicating a sleep state of said processor and said Power-Good signal line;
 - a mobile Voltage-Identification multiplexer for generating an MBL value from said input lines for indicating a default core voltage of said processor and said input lines for indicating a programmable core voltage requested by said processor according to said Power-Good signal line;
 - 15 a CPU-type multiplexer for generating a VIDOUT value from said MBL value and said DKTP value according to said input line for indicating a type of said processor; and
 - a Voltage-Identification override multiplexer for generating a value from said VIDOUT value and said value in said programmable VID override table.
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Claim 6 (original): The integrated circuit of claim 5, wherein said DKTP value equals said value of said input lines for indicating a default core voltage of said processor if said Power-Good signal line indicates suitable power conditions and said input line for indicating a sleep state of said processor indicates that said processor is not sleeping, otherwise said DKTP value equals said value of said default sleep Voltage lines.

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Claim 7 (original): The integrated circuit of claim 5, wherein said MBL value equals said value of said input lines for indicating a default core voltage of said processor if said Power-Good signal line does not indicate suitable power conditions, otherwise said MBL value equals said value of said input lines for indicating a programmable core voltage requested by said processor.

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Claim 8 (original): The integrated circuit of claim 5, wherein said VIDOUT value equals said MBL value if said input line for indicating a type of said processor indicates a mobile-type CPU, otherwise said VIDOUT value equals said DKTP value.

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Claim 9 (original): The integrated circuit of claim 5, wherein if any bits in a value of said programmable VID override table are zero, then said Voltage-Identified value equals said value of said programmable Voltage-Identified override table, otherwise said Voltage-Identified value equals said VIDOUT value.

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Claim 10 (original): The integrated circuit of claim 5 further comprising a Frequency-Identification logic circuit for providing a Frequency-Identification value to said North Bridge chipset or said South Bridge chipset, said Frequency-Identification logic circuit comprising a Frequency-Identification override multiplexer for generating said a Frequency-Identification value from said input lines for indicating a processor operating frequency and said value of said programmable FID override table

Claim 11 (original): The integrated circuit of claim 10, wherein if any bits in a value of said programmable Frequency-Identification override table are zero, then said Frequency-Identification value equals said value of said programmable Frequency-Identification override table, otherwise said Frequency-Identification value equals a value from said input lines for indicating a processor operating frequency.

Claim 12 (original): The integrated circuit of claim 5 wherein a first operational voltage is used by said input lines for indicating a programmable core voltage requested by said processor, said input lines for indicating a default core voltage of said processor, said input lines for indicating a processor operating frequency and said output lines for overriding a internal Frequency-Identified code of said processor, wherein a second operational voltage is used by said input line for indicating a type of said processor, said input line for indicating a sleep state of said processor, said serial data input line and said output lines for providing said Frequency-Identification

value to said North Bridge chipset or said South Bridge chipset, and
wherein a third operational voltage is used by said output lines for passing said
Voltage-Identification value to said power regulator.

- 5 Claim 13 (original): The integrated circuit of claim 12 wherein said first operational
voltage is 2.5V, said second operational voltage is 3.3V, and said third operational
voltage is 5.0V.

- 10 Claim 14 (original): The integrated circuit of claim 12 further comprising an output
line for indicating a default core voltage of said processor that utilizes said first
operational voltage, a value of said output line for indicating a default core voltage of
said processor being equal to a value of a most significant bit of said output lines for
passing said Voltage-Identification value to said power regulator.

- 15 Claim 15 (original): The integrated circuit of claim 12 further comprising an output
line for indicating a default core voltage of said processor that utilizes said second
operational voltage, a value of said output line for indicating a default core voltage of
said processor being equal to a value of a most significant bit of said output lines for
passing said Voltage-Identification value to said power regulator.

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